IN THE CLAIMS

Please cancel claim 38.

Please amend claims 33, 35, 39, 40, 43 and 45 as follows:

1.-32. (Cancelled).

33. (Currently Amended) An electrical test circuit for testing integrated circuits, particularly dynamic A/D converters, the electrical test circuit comprising:

a first input configured for receiving a test signal of an integrated circuit;

a ~~third~~ second input configured to receive a normalized reference signal, particularly one that

is formed to be synchronous with the test signal;

a control device configured such that a deviation or an amplitude or a phase of the reference signal or of the test signal is or, respectively, are changed;

~~a measuring~~ the control device configured to generate a difference signal by subtracting the reference signal from the test signal; ~~and~~

an output for outputting the difference signal; and

a measuring device configured to receive the difference signal;

wherein the control device comprises a control loop circuit which is provided for adapting the deviation of the test signal, the control loop circuit being configured in such a manner that a deviation-corrected test signal is generated in that the difference values between the deviation of the test signal and of the reference signal are added together to obtain an aggregate difference value and in that the test signal is corrected by addition with the aggregate difference value.

34. (Previously Presented) The electrical test circuit according to claim 33, wherein the measuring device is configured to generate at least one quality parameter from the difference signal.

35. (Currently Amended) The electrical test circuit according to claim 34, wherein the quality parameters are ~~the~~ a standard deviation of the test signal or the deviation of the test signal or the amplitude of the test signal.

36. (Previously Presented) The electrical test circuit according to claim 33, wherein the test signal, the reference signal, the difference signal and a quality parameter or parameters are present in digital form.

37. (Previously Presented) The electrical test circuit according to claim 33, wherein from the difference signal or from the quality parameter, a ratio between a signal and a noise component of the test signal or the ratio between the signal and the noise or distortion component of the test signal or a total unadjusted error of the test signal or the total adjusted error is calculated.

38. (Canceled)

39. (Currently Amended) An electrical test circuit for testing integrated circuits, particularly dynamic A/D converters, the electrical test circuit comprising:

a first input configured for receiving a test signal of an integrated circuit;

a ~~third~~ second input configured to receive a normalized reference signal, particularly one that is formed to be synchronous with the test signal;

a control device configured such that a deviation or an amplitude or a phase of the reference signal or of the test signal is or, respectively, are changed;

~~a measuring~~ the control device configured to generate a difference signal by subtracting the reference signal from the test signal; ~~and~~

an output for outputting the difference signal; and

a measuring device configured to receive the difference signal;

wherein the control device comprises an amplitude correction circuit for matching the amplitude of the reference signal to the amplitude of the test signal, the amplitude correction circuit being configured in such a manner that an amplitude-corrected reference signal is generated in that ~~the~~ an absolute value of the deviation-corrected test signal is determined and added together by the amplitude correction circuit to obtain an ~~a~~ aggregate absolute value of the deviation corrected test signal and in that the reference signal is corrected with the aggregate absolute value of the deviation-corrected test signal.

40. (Currently Amended) An electrical test circuit for testing integrated circuits, particularly dynamic A/D converters, the electrical test circuit comprising:

a first input configured for receiving a test signal of an integrated circuit;

a ~~third~~ second input configured to receive a normalized reference signal, particularly one that

is formed to be synchronous with the test signal;

a control device configured such that a deviation or an amplitude or a phase of the reference signal or of the test signal is or, respectively, are changed;

a measuring device configured to generate a difference signal by subtracting the reference signal from the test signal; and

an output for outputting the difference signal The wherein the control device comprises a phase displacement circuit, the phase displacement circuit being configured in such a manner that the phase of the reference signal is matched to the phase of the test signal.

41. (Previously Presented) The electrical test circuit according to claim 40, wherein the phase displacement circuit comprises a shift register, a decoder, at least one bus driver and at least one D-type flip flop.

42. (Previously Presented) The electrical test circuit according to claim 40, wherein the phase of the reference signal is displaced up to one half signal period by the phase displacement circuit.

43. (Currently Amended) An electrical test circuit for testing integrated circuits, particularly dynamic A/D converters, the electrical test circuit comprising:

a first input configured for receiving a test signal of an integrated circuit;

a ~~third~~ second input configured to receive a normalized reference signal, particularly one that is formed to be synchronous with the test signal;

a control device configured such that a deviation or an amplitude or a phase of the reference signal or of the test signal is or, respectively, are changed;

~~a measuring~~ the control device configured to generate a difference signal by subtracting the reference signal from the test signal; ~~and~~

an output for outputting the difference signal; and

a measuring device configured to receive the difference signal;

wherein squares of ~~the~~ amounts of difference values between a deviation-corrected test signal and an amplitude- and phase-corrected reference signal are added together by the measuring device or minimum and maximum values of the difference values between the deviation-corrected test signal and the amplitude- and phase-corrected reference signal are stored by the measuring device.

44. (Previously Presented) The electrical test circuit according to claim 43, wherein the electrical test circuit is configured in such a manner that a standard deviation is calculated by the measuring device from the square of the amounts of the difference values between the deviation-corrected test signal and the amplitude- and phase-corrected reference signal or from the minimum value of the difference values between the deviation-corrected test signal and the amplitude- and phase-corrected reference signal or from the maximum value of the difference

values between the deviation-corrected test signal and the amplitude- and phase-corrected reference signal.

45. (Currently Amended) The electrical test circuit according to claim 43, wherein the electrical test circuit is configured in such a manner that the phase of the reference signal is adjusted in accordance with a minimum of ~~the~~ a standard deviation by a phase displacement circuit.

46. (Withdrawn) An electrical phase displacement circuit for correcting the phase of a reference signal with respect to a test signal of an integrated circuit, the electrical phase displacement circuit comprising:

a first input, for receiving a reference signal from a tester;

a second input for receiving a clock pulse signal from a tester;

at least one bus driver which is coupled to at least one D-type flip flop;

the D-type flip flop or flip flops are provided for displacing the phase of the reference signal;

a shift register and a selection element coupled to the shift register, particularly a decoder, which is formed in such a manner that in each case one bus driver is activated in dependence on the data stored in the shift register,

a first output connected to the bus drivers, which is intended for sending out the phase-displaced reference signal; and

a second output which is intended for sending out a control signal.

47. (Previously Presented) An electrical circuit for the tolerance tube test of integrated circuits, particularly of dynamic A/D converters, the electrical circuit comprising:

an electrical test circuit as claimed in claim 40; and

an electrical phase displacement circuit configured such that the phase of the reference signal is adjusted in accordance with the minimum of the standard deviation;

a first output of the electrical phase displacement circuit being connected to the third input of the electrical test circuit and a second output of the electrical phase displacement circuit being connected to the second input of the electrical test circuit.

48. (Previously Presented) An integrated circuit comprising:

an electrical test circuit according claim 40; and

an electrical phase displacement circuit configured such that the phase of the reference signal is adjusted in accordance with the minimum of the standard deviation;.

49. (Previously Presented) A probe card for testing integrated circuits, the probe card comprising:

an electrical test circuit according to claim 40; and

an electrical phase displacement circuit comprising:

a first input, for receiving a reference signal from a tester;

a second input for receiving a clock pulse signal from a tester;

at least one bus driver which is coupled to at least one D-type flip flop;

the D-type flip flop or flip flops are provided for displacing the phase of the reference

signal;

a shift register and a selection element coupled to the shift register, particularly a decoder, which is formed in such a manner that in each case one bus driver is activated in dependence on the data stored in the shift register,

a first output connected to the bus drivers, which is intended for sending out the phase-displaced reference signal; and

a second output which is intended for sending out a control signal.

50. (Previously Presented) A load board for receiving a probe card for testing integrated circuits or with one or more test sockets for testing integrated circuits or for connecting a handler to a tester of integrated circuits, the load board comprising:

an electrical test circuit according to claim 40; and

an electrical phase displacement circuit comprising:

a first input, for receiving a reference signal from a tester;

a second input for receiving a clock pulse signal from a tester;

at least one bus driver which is coupled to at least one D-type flip flop;

the D-type flip flop or flip flops are provided for displacing the phase of the reference

signal;

a shift register and a selection element coupled to the shift register, particularly a decoder, which is formed in such a manner that in each case one bus driver is activated in dependence on the data stored in the shift register,

a first output connected to the bus drivers, which is intended for sending out the phase-displaced reference signal; and

a second output which is intended for sending out a control signal.

51. (Previously Presented) A tester with measuring sensors, particularly for currents and voltages, and with instruments for generating digital signals or data streams, the tester comprising:

one electrical test circuit according to claim 40; and

an electrical phase displacement circuit comprising

a first input, for receiving a reference signal from a tester;

a second input for receiving a clock pulse signal from a tester;

at least one bus driver which is coupled to at least one D-type flip flop;

the D-type flip flop or flip flops are provided for displacing the phase of the reference

signal;

a shift register and a selection element coupled to the shift register, particularly a decoder, which is formed in such a manner that in each case one bus driver is activated in dependence on the data stored in the shift register,

a first output connected to the bus drivers, which is intended for sending out the phase-displaced reference signal; and

a second output which is intended for sending out a control signal.

52. (Previously Presented) The tester according to claim 51, wherein a low-pass filter is provided which is configured in such a manner that the digital signal received by the low-pass filter or, respectively, the digital data stream received by the low-pass filter is converted into an analog signal.

53. (Previously Presented) A tester with measuring sensors, particularly for currents and voltages, and with instruments for generating analog signals, the tester comprising:

an electrical test circuit according to claim 40; and

an electrical phase displacement circuit comprising

a first input, for receiving a reference signal from a tester;

a second input for receiving a clock pulse signal from a tester;

at least one bus driver which is coupled to at least one D-type flip flop;

the D-type flip flop or flip flops are provided for displacing the phase of the reference

signal;

a shift register and a selection element coupled to the shift register, particularly a decoder, which is formed in such a manner that in each case one bus driver is activated in dependence on the data stored in the shift register,

a first output connected to the bus drivers, which is intended for sending out the phase-displaced reference signal; and

a second output which is intended for sending out a control signal.

54. (Withdrawn) A method for testing an integrated circuit, comprising:

equipping a tester with an integrated circuit;

applying current and voltage values to the integrated circuit by the tester;

generating a reference signal by means of the tester, which corresponds to the ideal output signal of the integrated circuit;

displacing the phase of the reference signal in such a manner that the reference signal and the test signal of the integrated circuit vary essentially synchronously;

matching the amplitude of the reference signal to the amplitude of the test signal;

matching the deviation of the test signal to the reference signal;

forming a difference signal by subtracting the reference signal from the test signal; and

evaluating the difference signal.

55. (Withdrawn) The method as claimed in claim 54, comprising wherein at least part of the method is performed with an electrical test circuit according to claim 33 and with an electrical phase displacement circuit according to claim 46.

56. (Withdrawn) The method according to claim 54, comprising wherein the electrical test circuit or the tester forms a quality value, particularly the standard deviation of the test signal or the deviation of the test signal or the amplitude of the test signal.

57. (Withdrawn) The method according to claim 54, comprising wherein the electrical test circuit or the tester determine the ratio between the signal and the noise component (SNR) or the ratio between the signal and the noise or distortion component (SNDR) or the total unadjusted error (TUE) or the total adjusted error (TAE).

58. (Withdrawn) The method according to claim 54, comprising wherein analog current and voltage values are applied to the integrated circuit by the tester.

59. (Withdrawn) The method according to claim 58, comprising wherein the tester additionally comprises a conversion unit, particularly a low-pass filter, which, converts a digital data stream generated by the tester into analog current and voltage values and applies these to the integrated circuit.

60. (Withdrawn) A computer program for executing a method for testing an electronic component, which is configured in such a manner that the method is executed according to claim 54.

61. (Withdrawn) The computer program as claimed in claim 60, comprising wherein it is contained on a storage medium, particularly in a computer memory or in a random access memory.

62. (Withdrawn) The computer program as claimed in claim 60 which is transmitted on an electrical carrier signal.

63. (Withdrawn) A data medium with a computer program as claimed in claim 60.

64. (Withdrawn) A method in which a computer program as claimed in claim 60 is downloaded from an electronic data network such as, for example, from the Internet to a computer connected to the data network.